



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor : **Atsushi NISHIZAWA**
Serial No : **09/751,979**
Filed : **January 23, 2001**
Title : **MANUFACTURING METHOD OF SEMICONDUCTOR...**
Group Art Unit : **1765**

May 4, 2001

Attn: Customer Corrections Division
Assistant Commissioner for Patents
Washington, D.C. 20231

RECEIVED
OCT 19 2001
TC 1700

REQUEST FOR CORRECTED FILING RECEIPT

SIR:

We received the filing receipt on the above-referenced case, copy enclosed,
wherein the **ASSIGNMENT FOR PUBLISHED PATENT APPLICATION** was incorrectly listed as: **NEC CORP.**
Please change the same to read: **NEC CORPORATION**. Also the **TITLE** was incorrectly listed as:
MANUFACTURING METHOD SEMICONDUCTOR INTERGRATED CIRCUIT INCLUDING
SIMULTANEOUS FORMATION OF VIA HOLE REACHING METAL WIRING AND CONCAVE GROOVE
IN INTERLAYTER.... Please change the same to read: **MANUFACTURING METHOD OF**
SEMICONDUCTOR INTERGRATED CIRCUIT INCLUDING SIMULTANEOUS FORMATION OF VIA
HOLE REACHING METAL WIRING AND CONCAVE GROOVE IN INTERLAYER FILM AND
SEMICONDUCTOR INTERGRATED CIRCUIT MANUFACTURED WITH THE MANUFACTURING
METHOD.

Any fee, due as a result of this paper not fully covered by an enclosed check, may
be charged on Deposit Account No. 08-1634.

Respectfully submitted,

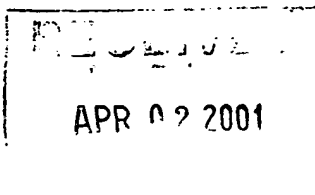
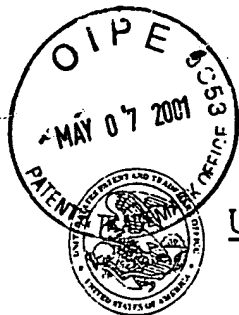
Samson Helfgott
Reg. No. 23,072

Helfgott & Karas, P.C.
60th Floor
Empire State Building
New York, New York 10118
Tel. (212) 643-5000
Docket No.: 18.159
SH:aju:FILREC

I HEREBY CERTIFY THAT THIS CORRESPONDENCE
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APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/751,979	12/29/2000	1765	710	NECW 18.159	6	12	2

CONFIRMATION NO. 9046

HELFGOTT & KARAS, P.C.
60th Floor
Empire State Building
New York, NY 10118-0110

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FILING RECEIPT



OC000000005913685

Date Mailed: 03/28/2001

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the PTO processes the reply to the Notice, the PTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Atsushi Nishizawa, Tokyo, JAPAN;

Assignment For Published Patent Application

NEC Corp.; CORPORATION

Continuing Data as Claimed by Applicant

Foreign Applications

JAPAN 2000-009221 01/18/2000

If Required, Foreign Filing License Granted 03/27/2001

Projected Publication Date: 07/19/2001

Non-Publication Request: No

Early Publication Request: No

Title

OF
Manufacturing method of Semiconductor integrated circuit including simultaneous formation of
via hole reaching metal wiring and concave groove in interlayer film and semiconductor
integrated circuit manufactured with the manufacturing method

INTERLAYER

Preliminary Class

438

Data entry by : IBRAHIM, SADIE

Team : OIPE

Date: 03/28/2001

